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DESIGN AND OPTIMIZATION OF REVERSIBLE CARRY LOOK AHEAD ADDER CIRCUIT

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ABSTRACT

Power dissipation is a prominent factor in limiting the chip area. Conventional computing has been facing many challenges from the last couple of decades. The device scaling versus technology has reached saturation, forcing the designers to look for alternative methods. Reversible design is a promising alternative to these limitations, with increasing applications such as nano-computing, quantum computing, low power dissipating digital designs, etc. Reversible logic promises the minimization or even elimination of power dissipation [1][2][3]. In this paper, the Carry Look-ahead Adder (CLA) circuit is designed using reversible logic. The proposed deigns are efficient compared to the existing designs in terms of gate counts, garbage outputs and quantum cost. The design can be extended to construct an n-bit adder circuit. Extension to a 16 bit adder is also shown in this paper. The results given in the paper show that the reversible designs dissipates very less power than the CMOS design. The 16-bit CLA using Toffoli gates dissipated 0.21% and design using Peres gates dissipated 0.27% compared to the power dissipated by conventional CMOS design.

KEYWORDS: Reversible Logic, Constant/Garbage Input, Garbage Output, Quantum Cost, CLA